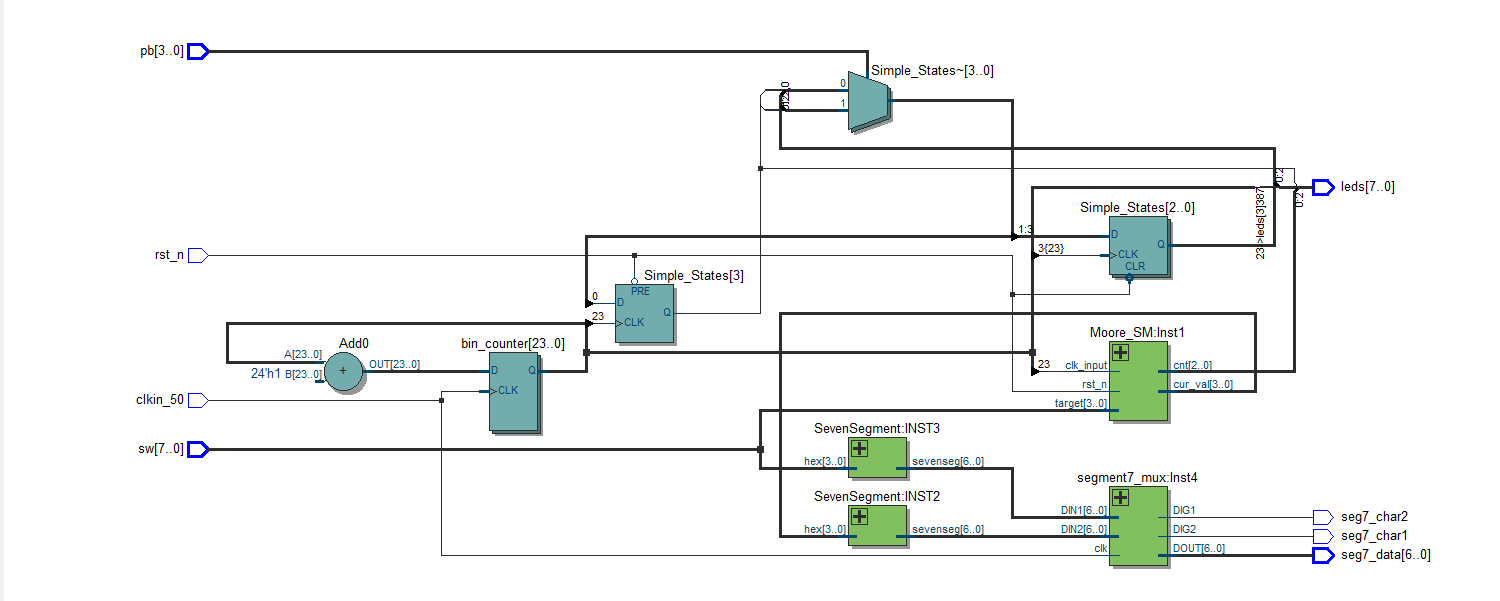
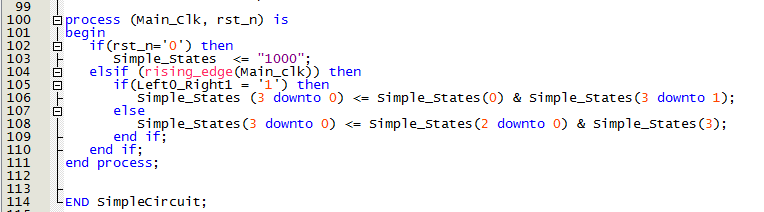
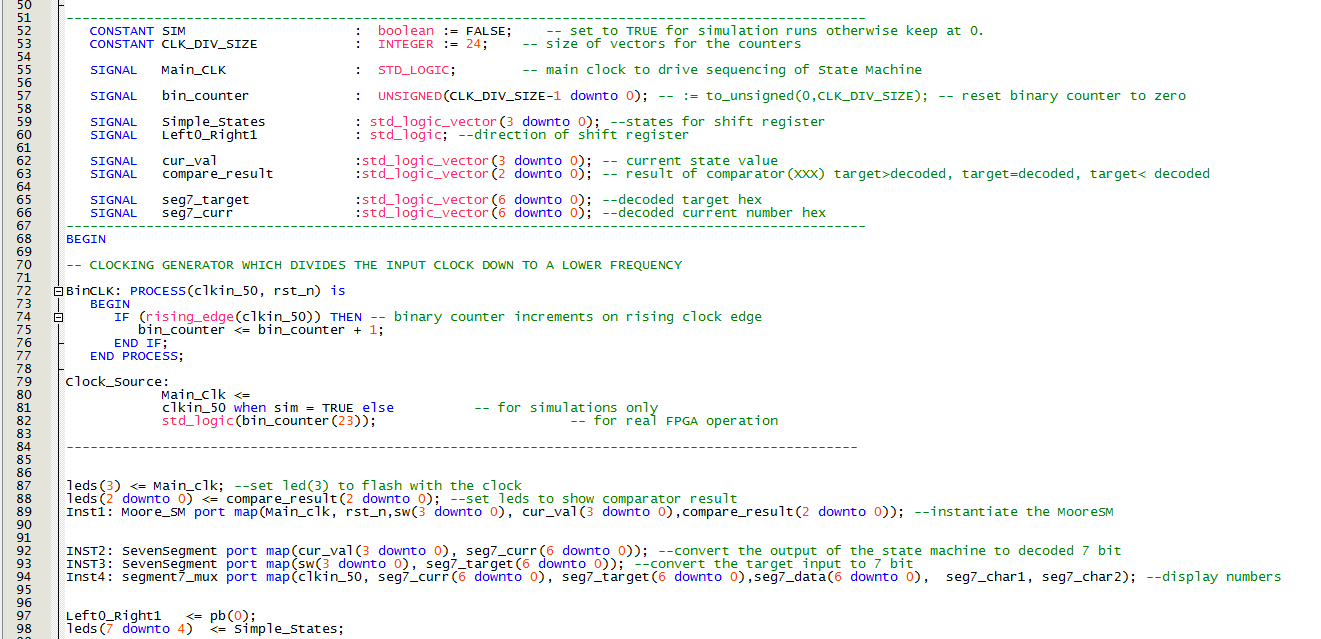
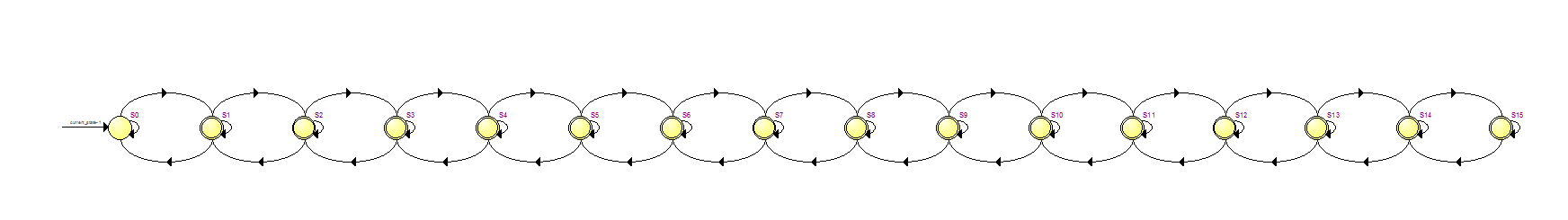
VHDL RTL View



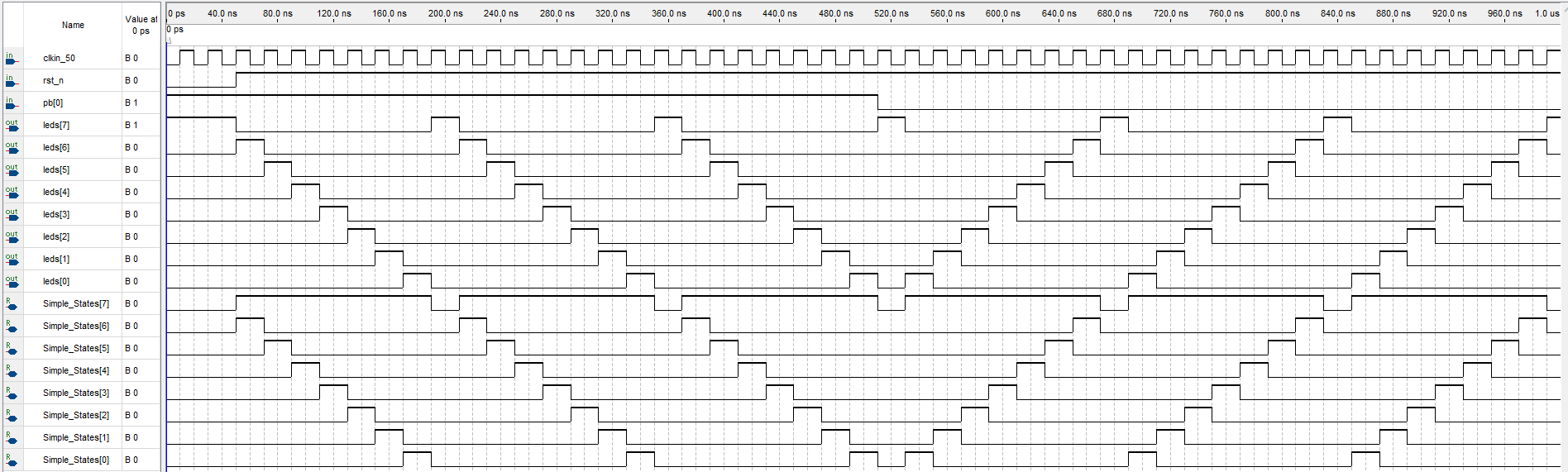


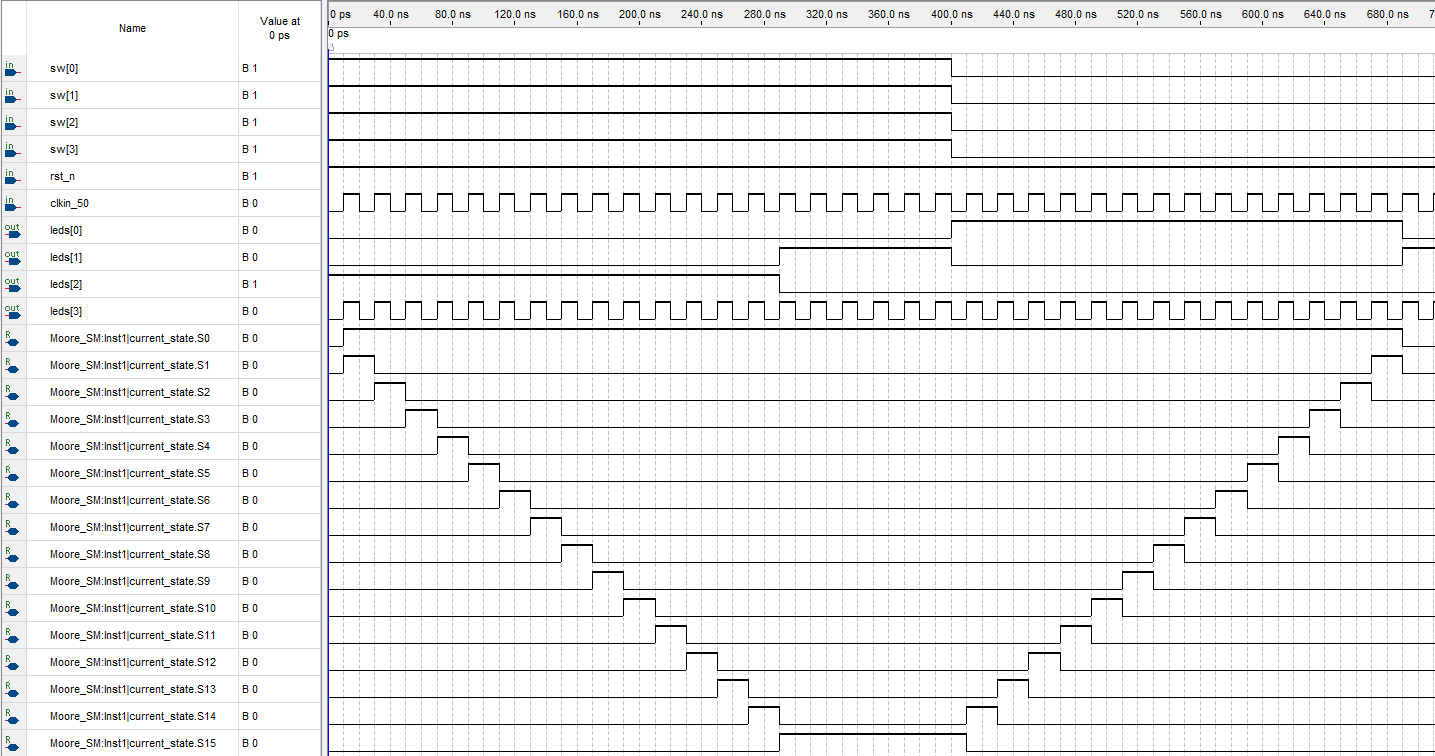


State machine diagram



Shift register simulation in both directions



Moore State Machine simulation 

Total logic elements used (103)

